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For: SINGLE INSTRUCTION MULTIPLE DATA ARRAY CELL

1 1. A single instruction multiple data (SIMD) array cell for processing a data stream,
2 said array including a plurality of cells, each cell comprising:

3 a memory circuit for storing a predetermined region of the data stream;

4 a location register circuit for representing the size and location of the
5 predetermined region of the data stream;

6 a unique identification number; and

7 an arithmetic logic unit responsive to said identification number and a
8 single command common to all cells in a load mode to compute the unique start position for its
9 cell for receiving the predetermined region of the direct memory access data stream.

1 2. The single instruction multiple data array of claim 1 in which said arithmetic logic
2 unit includes an adder circuit.

1 3. The single instruction multiple data array of claim 2 in which said adder circuit
2 includes a shifter circuit for performing in combination with said adder circuit multiplication and
3 accumulation.

1 4. The single instruction multiple data array of claim 1 in which said arithmetic logic
2 unit includes an arithmetic logic circuit.

1 5. The single instruction multiple data array of claim 1 in which the command word
2 in an execution mode includes an address field applicable to all cells and a data field and said
3 arithmetic logic unit operates directly on the value stored at that address in its cell's memory with
4 the data in the data field.

1 6. The single instruction multiple data array of claim 5 in which said command word
2 in said execution mode includes an instruction field for operating said arithmetic logic unit.

1 7. The single instruction multiple data array of claim 1 in which said arithmetic logic
2 unit includes a multiplexor for presenting inputs from said memory circuit, said command word,
3 said unique identification number, and the output of the arithmetic logic unit.

1 8. The single instruction multiple data array of claim 1 in which each said cell
2 includes a condition code register and said arithmetic logic unit responds to said unique
3 identification number and said condition code register to control the condition of the cell.

1 9. The single instruction multiple data array of claim 1 in which said location register
2 circuit stores a start position for the predetermined region to be stored in its memory, the length of
3 the direct memory access data stream to be stored and at least one dimension of the data stream.

1 10. The single instruction multiple data array of claim 9 in which said location register
2 circuit stores the vertical and horizontal dimension of the data stream.

11. The single instruction multiple data array of claim 1 in which said command word in the execution mode establishes the size and location of predetermined region in the location register circuit.

12. The single instruction multiple data array of claim 1 in which said command word includes an address field for addressing locations in said predetermined region of interest in said memory circuit.

13. The single instruction multiple data array of claim 6 in which said command word in said execution mode includes a data field for operating said arithmetic logic unit.

14. The single instruction multiple data array of claim 5 in which each said cell includes a condition code register and said arithmetic logic unit responds to said unique identification number, said data field, and said condition code register to control the condition of the cell.